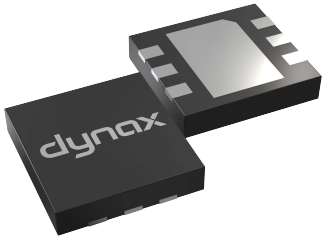
# DXG2PH36A-100N

## RF Power GaN Transistor




## 1. Product profile

### 1.1 General description

DXG2PH36A-100N is a 100 W RF GaN HEMT Transistor with second generation RF GaN technology from Dynax, which is ideal for cellular base station applications at frequencies from 3300 MHz to 3800 MHz.

**Table 1. Typical performance [1]**

| Freq (MHz) | $P_{sat}$ [2] (dBm) | $P_{avg}$ [3] (dBm) | $\eta_D$ [3] (%) | $G_P$ [3] (dB) | ACPR [3] (dBc) |
|---|---|---|---|---|---|
| 3400 | 50.4 | 41.3 | 53.4 | 15.8 | -30.0 |
| 3500 | 50.2 | 41.3 | 54.3 | 15.8 | -32.0 |
| 3600 | 50.0 | 41.3 | 53.6 | 15.2 | -33.0 |

[1] Typical Doherty performance in Dynax Demo with the device soldered onto the heatsink, test condition: $V_{DS}$ = 48 V, $I_{DQA}$ = 90 mA , $V_{GSB}$ = - 5.2 V.

[2] Test condition: Input signal Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ±5 MHz offset.

### 1.2 Features and benefits

- High efficiency, high gain
- Internally matched for broadband performance
- Designed for Digital Pre-Distortion error correction systems
- Optimized for Doherty applications

### 1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 3300 MHz to 3800 MHz frequency range

### 1.4 Lead-free and RoHS compliant

Pb RoHS

## 2. Pinning information

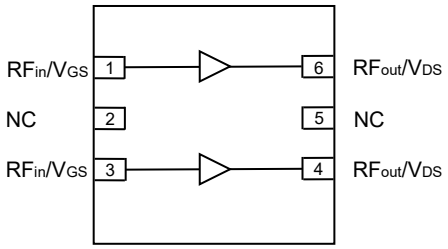



Fig 1. Pin configuration (Top view)

## 3. Ordering information

### Table 2. Ordering information

| Part number | Marking | Package type | Packaging information |
|---|---|---|---|
| DXG2PH36A-100N | DS10C | DFN 7×6.5mm | Tray: Suffix = 416 units |
| | | | Tape and Reel：Suffix = 1000 units；16 mm Tape width；13-inch Reel |

## 4. Maximum ratings

### Table 3. Maximum ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 150 | V |
| Gate-Source Voltage | $V_{GS}$ | -10 ~ +2 | V |
| Operating Voltage | $V_{DS}$ | 0 ~ +55 | V |
| Maximum Forward Gate Current | $I_{GMAX}$ | 10.4 | mA |
| Storage Temperature Range | $T_{STG}$ | - 65 ~ +150 | ℃ |
| Operating Junction Temperature | $T_J$ | 225 | ℃ |
| Absolute Maximum Channel Temperature [1] | $T_{MAX}$ | 275 | ℃ |

[1] Functional operation above 225℃ has not been characterized and is not implied. Operation at $T_{MAX}$ (275℃) reduces median time to failure by an order of magnitude; Operation beyond $T_{MAX}$ could cause permanent damage.

## 5. Thermal characteristics

### Table 4. Thermal characteristics

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| **Side A, Carrier** | | | |
| Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, $P_D$ = 11.4 W | $R_{thjc}$(IR) | 4.4 | ℃/W |
| Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, $P_D$ = 11.4 W | $R_{thjc}$(FEA) | 6.7 | ℃/W |
| **Side B, Peaking** | | | |
| Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, $P_D$ = 2.8 W | $R_{thjc}$(IR) | 2.1 | ℃/W |
| Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, $P_D$ = 2.8 W | $R_{thjc}$(FEA) | 3.7 | ℃/W |

## 6. ESD protection characteristics

### Table 5. ESD protection characteristics

| Test Methodology | Class |
|---|---|
| Human Body Model (per JS-001-2012) | 1A (≥ 250 V) |
| Charged Device Model (per JESD22-C101F) | C3 (≥ 1000 V) |

## 7. Moisture sensitivity level

### Table 6. Moisture sensitivity level

| Test Methodology | Class |
|---|---|
| Moisture Sensitivity Level (per J-STD-020) | Level 3 |

## 8. Electrical characteristics (TA = 25℃ unless otherwise noted)

### Table 7. DC characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Side A, Carrier** | | | | | |
| Drain-Source Leakage Current ($V_{GS}$ = -10 V, $V_{DS}$ = 150 V) | $I_{DSS}$ | - | - | 4.0 | mA |
| Drain-Source Breakdown Voltage ($V_{GS}$ = -10 V, $I_D$ = 4.0 mA) | $V_{(BR)DSS}$ | 150 | - | - | V |
| Gate Threshold Voltage ($V_{DS}$ = 48 V, $I_D$ = 4.0 mA) | $V_{GS(th)}$ | -4.0 | -3.3 | -1.0 | V |
| Gate Quiescent Voltage ($V_{DS}$ = 48 V, $I_D$ = 100 mA) | $V_{GS(Q)}$ | - | -3.0 | - | V |
| **Side B, Peaking** | | | | | |
| Drain-Source Leakage Current ($V_{GS}$ = -10 V, $V_{DS}$ = 150 V) | $I_{DSS}$ | - | - | 6.4 | mA |
| Drain-Source Breakdown Voltage ($V_{GS}$ = -10 V, $I_D$ = 6.4 mA) | $V_{(BR)DSS}$ | 150 | - | - | V |
| Gate Threshold Voltage ($V_{DS}$ = 48 V, $I_D$ = 6.4 mA) | $V_{GS(th)}$ | -4.0 | -3.3 | -1.0 | V |
| Gate Quiescent Voltage ($V_{DS}$ = 48 V, $I_D$ = 150 mA) | $V_{GS(Q)}$ | - | -3.0 | - | V |

### Table 8. RF characteristics (Typical Doherty performance – 3700 MHz) [1]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Peak Output Power [2] | $P_{sat}$ | 48.0 | 49.0 | - | dBm |
| Drain Efficiency [3] | $\eta_D$ | 40.0 | 47.0 | - | % |
| Power Gain [3] | $G_P$ | 12.9 | 14.5 | 16.1 | dB |

[1] Typical Doherty performance in Dynax DXG2PH36A-100N production test fixture, test condition: $V_{DS}$ = 48 V, $I_{DQA}$ = 60mA, $V_{GSB}$ = -2.1 V + $V_{GSQ}$ @15 mA.

[2] Test condition: Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: $P_{avg}$ = 41.3 dBm, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF.

### Table 9. Load mismatch

| Parameter | Result |
|---|---|
| VSWR 10:1 at $V_{DS}$ = 48 V,<br>100 W Pulsed CW output power,<br>Pulse width = 100 µs, Duty cycle = 10%. | No device damage |

# 9. Test information

## 9.1 Typical application circuit

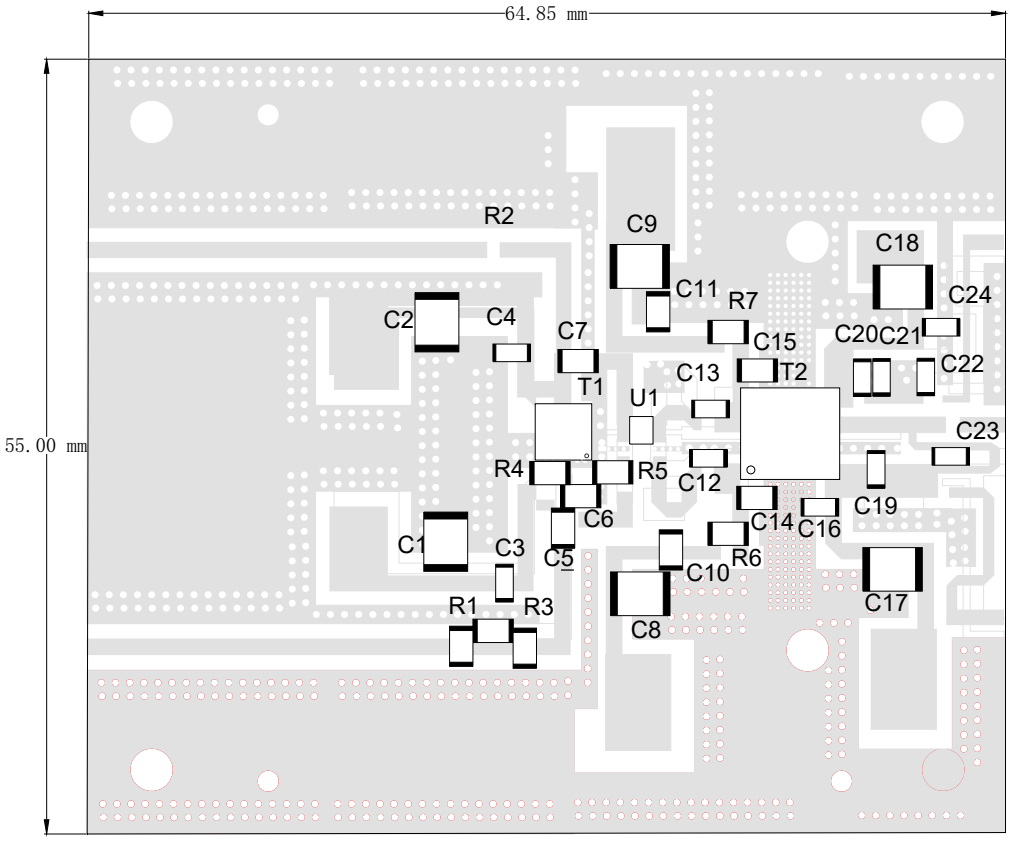



Fig 2. Component layout

**Table 10. List of components**

| S/N | Type | Designator | Description | Value | Vendor |
|---|---|---|---|---|---|
| 1 | Cap | C1,C2,C8,C9,C17,C18 | GRM32ER72A225KA | 2.2 uF | Murata |
| 2 | Cap | C3,C4,C7,C10,C11,C16,C23,C24 | ATC600F5R6JT250XT | 5.6 pF | ATC |
| 3 | Cap | C5 | ATC600F2R0JT250XT | 2.0 pF | ATC |
| 4 | Cap | C13 | ATC600F1R5JT250XT | 1.5 pF | ATC |
| 5 | Cap | C12 | ATC600F1R2JT250XT | 1.2 pF | ATC |
| 6 | Cap | C14 | ATC600F0R9JT250XT | 0.9 pF | ATC |
| 7 | Cap | C15 | ATC600F0R6JT250XT | 0.6 pF | ATC |
| 8 | Cap | C6,C20,C21,C22 | ATC600F0R3JT250XT | 0.3 pF | ATC |
| 9 | Cap | C19 | ATC600F0R1JT250XT | 0.1 pF | ATC |
| 10 | Res | R1,R3 | RC0805FR_07431RL | 431 Ω | Yageo |
| 11 | Res | R5 | RC0805FR_0750RL | 50 Ω | Yageo |
| 12 | Res | R2 | RC0805FR_0712RL | 12 Ω | Yageo |
| 13 | Res | R4,R6,R7 | RC0805FR_0710RL | 10 Ω | Yageo |
| 14 | Hybrid Coupler | U1 | C3337J5003AHF | 3 dB | Anaren |
| 15 | Transistor | T1 | DXG2PH60B-14N | / | Dynax |
| 16 | Transistor | T2 | DXG2PH36A-100N | / | Dynax |
| 17 | PCB | / | Rogers 4350B | 20 mil | Rogers |

## 9.2 Graphic data

### 9.2.1 Pulsed CW

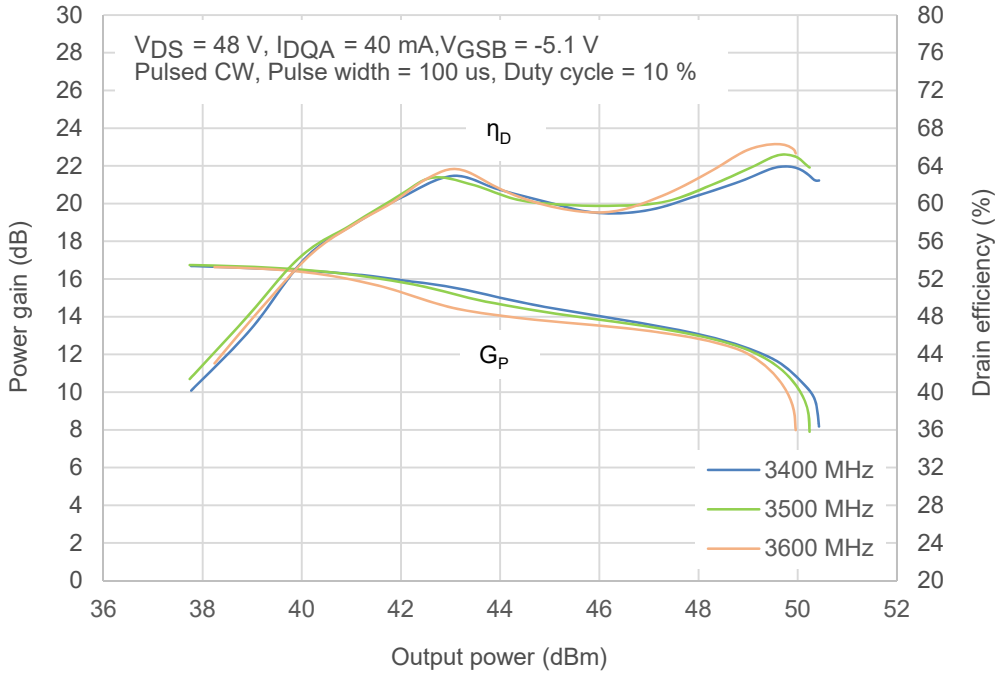



Fig 3. Power gain, Drain efficiency vs. Pulse output power

# 10. Impedance information

## 10.1 Impedance information

**Table 11. Typical impedance of carrier [1]**

| Maximum Output Power | | | | | | |
|---|---|---|---|---|---|---|
| Freq (MHz) | $Z_S$ (Ω) | $Z_L$ (Ω) | $G_P$ (dB) | $P_{sat}$ (dBm) | $P_{sat}$ (W) | $\eta_D$ (%) |
| 3400 | 11.0 - j24.5 | 7.7 - j3.5 | 19.5 | 46.3 | 42.6 | 69.2 |
| 3600 | 12.6 - j32.0 | 8.1 - j5.4 | 20.4 | 46.2 | 41.8 | 70.1 |
| 3800 | 18.8 - j24.4 | 7.6 - j8.4 | 20.0 | 46.2 | 41.8 | 68.4 |
| **Maximum Drain Efficiency** | | | | | | |
| Freq (MHz) | $Z_S$ (Ω) | $Z_L$ (Ω) | $G_P$ (dB) | $P_{sat}$ (dBm) | $P_{sat}$ (W) | $\eta_D$ (%) |
| 3400 | 11.0 - j24.5 | 5.2 + j2.9 | 21.1 | 44.4 | 27.5 | 77.6 |
| 3600 | 12.6 - j32.0 | 5.8 + j0.7 | 21.8 | 44.1 | 25.7 | 78.7 |
| 3800 | 18.8 - j24.4 | 5.8 - j2.6 | 21.4 | 44.7 | 29.5 | 78.1 |

**Table 12. Typical impedance of peaking [2]**

| Maximum Output Power | | | | | | |
|---|---|---|---|---|---|---|
| Freq (MHz) | $Z_S$ (Ω) | $Z_L$ (Ω) | $G_P$ (dB) | $P_{sat}$ (dBm) | $P_{sat}$ (W) | $\eta_D$ (%) |
| 3400 | 13.4 - j35.4 | 5.2 - j9.2 | 21.1 | 48.7 | 74.1 | 72.6 |
| 3600 | 34.5 - j25.0 | 6.0 - j11.0 | 21.3 | 48.2 | 66.0 | 69.7 |
| 3800 | 13.2 - j8.8 | 5.4 - j12.8 | 21.3 | 48.3 | 67.6 | 71.3 |
| **Maximum Drain Efficiency** | | | | | | |
| Freq (MHz) | $Z_S$ (Ω) | $Z_L$ (Ω) | $G_P$ (dB) | $P_{sat}$ (dBm) | $P_{sat}$ (W) | $\eta_D$ (%) |
| 3400 | 13.4 - j35.4 | 5.0 - j6.9 | 21.9 | 48.1 | 64.5 | 76.7 |
| 3600 | 34.5 - j25.0 | 5.1 - j8.1 | 22.0 | 47.5 | 56.2 | 75.0 |
| 3800 | 13.2 - j8.8 | 5.0 - j9.3 | 21.4 | 47.1 | 51.2 | 76.6 |

[1] $V_{DS}$ = 48 V, $I_{DQA}$ = 100 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[2] $V_{DS}$ = 48 V, $I_{DQB}$ = 150 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

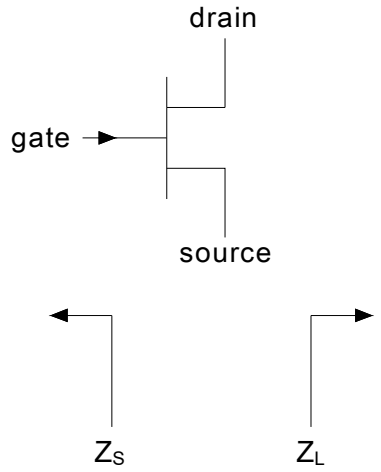



Fig 4. Definition of transistor impedance

## 11. Median lifetime

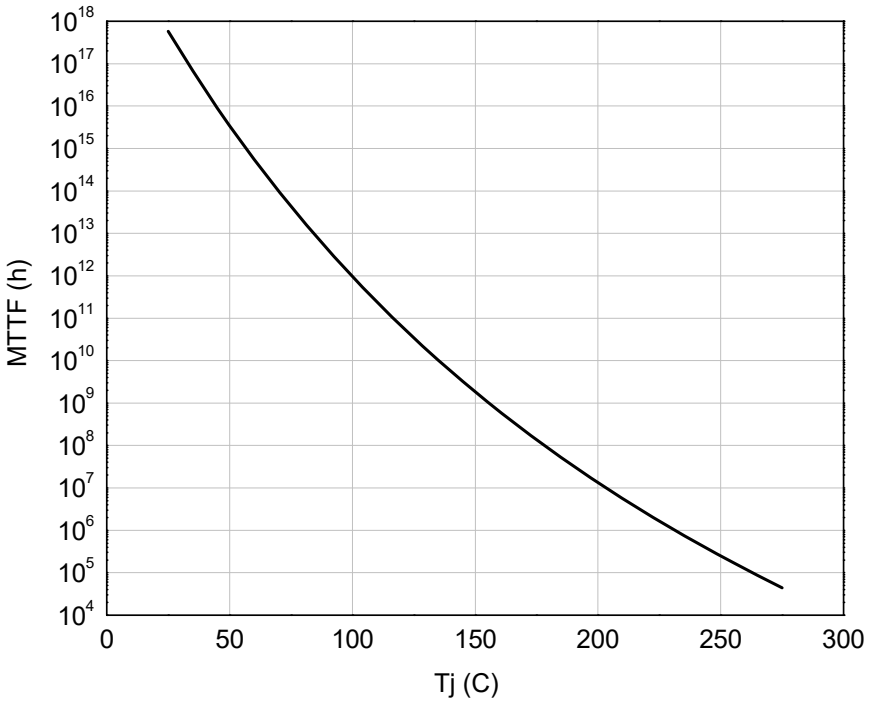



Fig 5. Median lifetime vs. channel temperature

## 12. Package outline

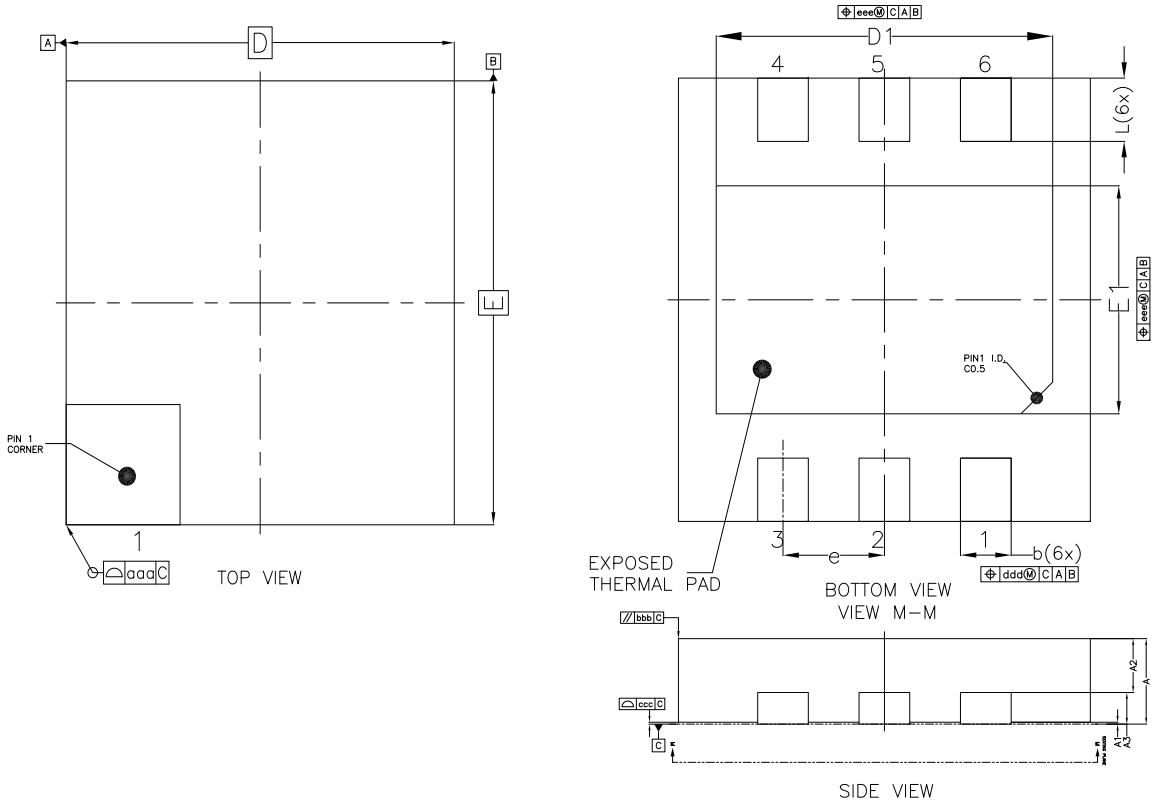



Fig 6. Package outline —— DFN 7×6.5mm

### Table 13. Package dimensions

| DESCRIPTION | | DIM | MILLIMETER | | |
|---|---|---|---|---|---|
| | | | MIN | NOM | MAX |
| TOTAL THICKNESS | | A | 1.30 | 1.35 | 1.40 |
| STAND OFF | | A1 | 0.00 | ----- | 0.05 |
| MOLD THICKNESS | | A2 | 0.80 | 0.85 | 0.90 |
| L/F THICKNESS | | A3 | 0.50 REF | | |
| BODY SIZE | X | D | 6.43 | 6.50 | 6.57 |
| | Y | E | 6.93 | 7.00 | 7.07 |
| LEAD PITCH | | e | 1.60 BSC | | |
| LEAD WIDTH | | b | 0.75 | 0.80 | 0.85 |
| LEAD LENGTH | | L | 0.95 | 1.00 | 1.05 |
| EP SIZE | | D1 | 5.26 | 5.31 | 5.36 |
| | | E1 | 3.55 | 3.60 | 3.65 |
| Tolerance of form and position | | | | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| LEAD COPLANARITY | | ccc | 0.08 | | |
| LEAD POSITION OFFSET | | ddd | 0.1 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

# 13. Abbreviations

**Table 14. Abbreviations**

| Acronym | Description |
|---|---|
| CW | Continuous Waveform |
| ESD | Electro-Static Discharge |
| GaN | Gallium Nitride |
| HEMT | High Electron Mobility Transistor |
| MTTF | Median Time To Failure |
| VSWR | Voltage Standing Wave Ratio |

# 14. Legal information

## 14.1 Datasheet status

| Document status | Product status | Definition |
|---|---|---|
| Objective [short] datasheet | Engineering sample | This document contains data from the objective specification for product development. |
| Preliminary [short] datasheet | Engineering sample | This document contains data from the preliminary specification. |
| Production [short] datasheet | Mass product | This document contains the product specification. |

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